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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Yeo, *et al.* Docket No.: TSM03-0553  
Serial No.: 10/667,871 Art Unit: 2811  
Filed: September 22, 2003 Examiner: TBD  
For: Resistor With Reduced Leakage

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Respectfully submitted,

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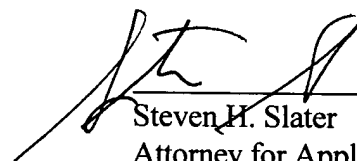
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The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & 08B that may be considered material to the examination of the above-identified application.

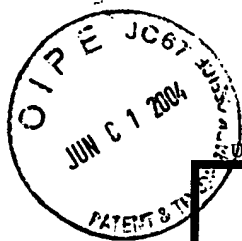
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Respectfully submitted,

May 26, 2004  
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<b>Substitute for form 1449/PTO</b>				<b>Complete if Known</b>	
				Application Number	10/667,871
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				Filing Date	September 22, 2003
				First Named Inventor	Yeo, et al.
				Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0553
Sheet	1	of	3		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
	1	US-4,631,803	12-30-1986	Hunter, et al.	
	2	US-4,946,799	08-07-1990	Blake, et al.	
	3	US-5,447,884	09-05-1995	Fahey, et al.	
	4	US-5,461,250	10-24-1995	Burghartz, et al.	
	5	US-5,534,713	07-09-1996	Ismail, et al.	
	6	US-5,714,777	02-03-1998	Ismail, et al.	
	7	US-5,763,315	06-09-1998	Benedict, et al.	
	8	US-6,046,487	04-04-2000	Benedict, et al.	
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	10	US-6,222,234 B1	04-24-2001	Imai	
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	13	US-2002/0076899 A1	06-20-2002	Skotnicki, et al.	
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	22	US-6,653,700 B2	11-25-2003	Chau, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
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				Application Number	10/667,871
				Filing Date	September 22, 2003
				First Named Inventor	Yeo, <i>et al.</i>
				Group Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0553
Sheet	2	of	3		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	23	ISMAIL, K., <i>et al.</i> , "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.	
	24	NAYAK, D.K., <i>et al.</i> , "Enhancement-Mode Quantum-Well Ge <sub>x</sub> Si <sub>1-x</sub> PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.	
	25	GAMIZ, F., <i>et al.</i> , "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.	
	26	GAMIZ, F., <i>et al.</i> , "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, (July 1, 2002), pp. 288-295.	
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	32	TIWARI, S., <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, (1997), pp.939-941.	
	33	OOTSUKA, F., <i>et al.</i> , "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meeting, (2000), pp. 575-578.	
	34	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers – I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, (1974), pp. 118-125.	
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Examiner Signature		Date Considered	

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	36	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	37	SCHÜPPEN, A., <i>et al.</i> , "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
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	43	YANG, F.L., <i>et al.</i> , "25 nm CMOS Omega FETs," IEDM 2002, pp. 255-258.	
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